REDUCED AREA OF CROSSBAR AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

There is disclosed a multi-processor system and method arranged, in one embodiment, as an image and graphics processor. The image processor is structured with several individual processors all having communication links to several memories. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

/32350/6470/ (P/REDUCED.ARE)